AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A system ~~for maintaining translation consistency in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host instruction set~~ comprising:

~~hardware~~ means for providing an indication whether a first memory address to be written stores a target instruction for a first instruction set architecture which has been translated to at least one host instruction for a second instruction set architecture, the at least one host instruction ~~that is~~ stored at a second memory address, ~~the at least one host instruction for execution by the host processor,~~ the ~~hardware~~ means for providing comprising:

a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses including a first storage location for the first memory address, and

a storage position corresponding to the first ~~in each~~ storage location ~~of the look-aside buffer~~ for storing the indication; and

~~software~~ means for responding to the indication and for assuring that the at least one host instruction will not be utilized once the first memory address has been written, in which case the ~~software~~ means for responding removes the at least one host instruction from the second memory address.

2. (Canceled).

3. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 1 in which the ~~software~~ means for responding

invalidates the at least one host instruction by marking the at least one host instruction at the second memory address.

4-17. (Canceled).

18. (Currently Amended) A memory controller comprising:

an address translation buffer including a plurality of storage locations in which recently accessed virtual addresses are to be recorded and in which physical addresses represented by the virtual addresses are to be recorded, each of the storage locations including means for indicating whether a physical address stores an instruction of a target instruction set which has been translated to an instruction of a host instruction set for execution by a computer system including a host processor, the instruction of the [[a]] host instruction set for execution by the memory controller; and

means for detecting an indication in a storage location to prevent a write access of the physical address and for indicating a subsequent operation before accessing the physical address, the means for detecting comprising:

means for generating an exception in response to the detection of the indication; and

means for responding to the exception to indicate the subsequent operation to be taken with respect to the instruction of a host instruction set before accessing the physical address.

19. (Canceled).

20. (Previously Presented) The memory controller as claimed in Claim 18 in which the means for indicating comprises a storage position in the storage location.

21. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 1 wherein the indication comprises a first bit value ~~associated with each of the storage locations in the look-aside buffer~~.

22. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 21 wherein a second bit value is also associated with the first storage location ~~each of the storage locations in the look-aside buffer~~, the second bit value for indicating a type for a respective physical address [[,]] ~~wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address~~.

23. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 1 wherein the host processor is a very long instruction word processor and wherein the target instruction set architecture comprises ~~instructions comprise~~ x86 instructions.

24. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 1 further comprising means for detecting the indication to prevent writing the first memory address and for indicating a subsequent operation before accessing the first memory address.

25. (Currently Amended) The system ~~for maintaining translation consistency~~ as claimed in Claim 24 wherein the means for detecting comprises:

means for generating an exception in response to the detection of the indication; and

means for responding to the exception to indicate the subsequent operation to be taken with respect to ~~the instruction of~~ the host instruction ~~set~~ before accessing the first memory address.

26. (Original) The memory controller as claimed in Claim 18 wherein the indication comprises a first bit value.

27. (Original) The memory controller as claimed in Claim 26 wherein a second bit value is also associated with the storage location, the second bit value for indicating a type for the physical address, wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

28. (Original) The memory controller as claimed in Claim 18 wherein the host processor is a very long instruction word processor and wherein the target instruction comprises an x86 instruction.

29. (New) The system as claimed in Claim 22 wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

30. (New) A computer-implemented method comprising:

checking a storage position for an indication whether a first memory address to be written stores a target instruction for a first instruction set architecture that has been translated to a host instruction for a second instruction set architecture, wherein the host instruction is executable by a host processor and is stored at a second memory address; and

preventing utilization of the host instruction subsequent to a write to the first memory address that overwrites the target instruction.

31. (New) The method as claimed in Claim 30 wherein the storage position is associated with a storage location for the first memory address in a look-aside buffer, wherein the look-aside buffer comprises a plurality of storage locations for virtual addresses and associated physical addresses.

32. (New) The method as claimed in Claim 31 wherein the indication comprises a first bit value, wherein a second bit value is also associated with the first memory address to indicate a type of physical address associated with the storage location.

33. (New) The method as claimed in Claim 32 wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

34. (New) The method as claimed in Claim 30 further comprising:

detecting an attempt to write to the first memory address;

generating an exception in response to the attempt to write; and

suspending the write to the first memory address until after the exception is handled.

35. (New) The method as claimed in Claim 34 further comprising removing the host instruction from the second memory address in response to the exception.

36. (New) The method as claimed in Claim 34 further comprising invalidating the host instruction in response to the exception.

37. (New) A computer system comprising:

a memory; and

a microprocessor coupled to the memory, the microprocessor comprising a look-aside buffer comprising a plurality of storage locations for virtual addresses and associated physical addresses including a first storage location for a first memory address; wherein the look-aside buffer comprises a configuration to indicate whether a first memory address to be written stores a target instruction for a first instruction set architecture that has been translated to a host instruction for a second instruction set architecture and that is stored at a second memory address, the host instruction for execution by the microprocessor; and wherein, in response to an indication that the first memory address to be written stores a target instruction that has been translated to a host instruction, the host instruction will not be utilized once the target instruction at the first memory address has been overwritten.

38. (New) The computer system as claimed in Claim 37 wherein the indication comprises a first bit value.

39. (New) The computer system as claimed in Claim 38 wherein a second bit value is also associated with the first storage location, wherein the second bit value indicates a type of physical address associated with the storage location for the first memory address.

40. (New) The computer system as claimed in Claim 39 wherein the type is selected from the group consisting of: a memory address; and a memory-mapped I/O address.

41. (New) The computer system as claimed in Claim 37 wherein, in response to detecting an attempt to write to the first memory address, an exception is generated in response to the attempt to write, wherein further the host instruction is removed from the second memory address in response to the exception and wherein the attempt to write is suspended until after the exception is handled.

42. (New) The computer system as claimed in Claim 37 wherein, in response to detecting an attempt to write to the first memory address, an exception is generated in response to the attempt to write, wherein further the host instruction is invalidated in response to the exception and wherein the attempt to write is suspended until after the exception is handled.